AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a wireless transceiver coupled to a programmable logic circuit, wherein (i) said programmable logic circuit comprises a programmable logic device, a processor, and a memory circuit in a single integrated circuit (IC) package, ~~and~~ (ii) said programmable logic device, said processor, and said memory circuit are coupled together and (iii) said processor is configured to communicate with a host system via said wireless transceiver and to program said programmable logic device via an interface configured to couple said processor and said programmable logic device.

2. (ORIGINAL) The apparatus according to claim 1, wherein said single integrated circuit package contains one or more integrated circuit dies.

3. (ORIGINAL) The apparatus according to claim 1, wherein said integrated circuit comprises a JEDEC standard integrated circuit package.

4. (ORIGINAL) The apparatus according to claim 1, wherein said wireless transceiver is contained within said package.

5. (ORIGINAL) The apparatus according to claim 1, wherein said wireless transceiver communicates using either electromagnetic or ultrasonic waves.

6. (ORIGINAL) The apparatus according to claim 5, wherein said electromagnetic waves comprise radio signals or infrared light.

7. (ORIGINAL) The apparatus according to claim 1, wherein said wireless transceiver communicates through a device selected from the group consisting of an antenna, a light emitting/sensitive device, and an ultrasonic transducer.

8. (ORIGINAL) The apparatus according to claim 7, wherein said light emitting/sensitive device comprises an infrared diode or other type or wavelength of light emitting/sensitive diode or transistor.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said processor and said programmable logic device are implemented on a single die.

10. (ORIGINAL) The apparatus according to claim 1, wherein said processor is selected from the group consisting of a

microprocessor, a micro-controller or other processor, a digital signal processor, and instructions stored in said memory circuit for configuring said programmable logic circuit as a processor.

11. (ORIGINAL) The apparatus according to claim 10, wherein said instructions configure said programmable logic device as a device selected from the group consisting of a microprocessor, a micro-controller, and a digital signal processor.

12. (ORIGINAL) The apparatus according to claim 1, wherein said memory circuit comprises one or more non-volatile memory elements.

13. (ORIGINAL) The apparatus according to claim 1, wherein said programmable logic device comprises one or more memory elements.

14. (ORIGINAL) The apparatus according to claim 13, wherein said memory elements are non-volatile.

15. (CURRENTLY AMENDED) A method for programming a programmable logic device using a wireless link comprising the steps of:

(A) presenting programming signals to a wireless transceiver; and

(B) programming a programmable logic circuit in response to said programming signals, wherein (i) said programmable logic circuit comprises a programmable logic device, a memory circuit, and a processor in a single integrated circuit package, ~~and~~ (ii) said programmable logic device, said processor, and said memory circuit are coupled together and (iii) said processor is configured (a) to communicate with a host system via said wireless transceiver and (b) to program said programmable logic device in response to said programming signals via an interface coupling said processor and said programmable logic device.

16. (ORIGINAL) The method according to claim 15, wherein said wireless transceiver is contained in said integrated circuit package.

17. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the steps of:

(C) during a first bootup, configuring said programmable logic device as said processor in response to instructions stored in said memory circuit; and

(D) reprogramming said memory circuit in response to said programming signals.

18. (CURRENTLY AMENDED) An apparatus comprising:

a programmable logic device;

a memory circuit;

a processor;

a first interface configured to couple said processor to said programmable logic device; and

a wireless transceiver, wherein (a) said programmable logic device, said memory circuit, and said processor are (i) encased in a single integrated circuit (IC) package and (ii) coupled together and (b) said processor is configured (i) to communicate with a host system via said wireless transceiver and (ii) to program said programmable logic device.

19. (ORIGINAL) The apparatus according to claim 18, wherein said wireless transceiver is contained within said integrated circuit package.

20. (ORIGINAL) The apparatus according to claim 18, further comprising a transducer coupled to said wireless transceiver.

21. (CURRENTLY AMENDED) The apparatus according to claim 18, further comprising:

~~an~~ a second interface configured to couple said programmable logic device with said memory circuit, wherein said programmable logic device is configured by said memory circuit during bootup.

22. (CURRENTLY AMENDED) The apparatus according to claim 18, further comprising:

~~an~~ a second interface configured to couple said processor with said memory circuit, wherein said processor is configured to perform one or more of (i) programming said memory circuit, (ii) reading said memory circuit, (iii) verifying said memory circuit and (iv) erasing said memory circuit.

23. (CANCELED)

24. (CURRENTLY AMENDED) The apparatus according to claim 18, further comprising:

a ~~first~~ second interface configured to couple said programmable logic device with said memory circuit, wherein said programmable logic device is configured by said memory circuit during bootup; and

a ~~second~~ third interface configured to couple said processor with said memory circuit~~; and~~

~~a third interface configured to couple said processor to said programmable logic device~~, wherein said processor is <u>further</u> configured ~~(a) to communicate with a host system via said wireless transceiver and (b)~~ to perform one or more of (i) programming said memory circuit, (ii) reading said memory circuit, (iii) verifying said memory circuit, <u>and</u> (iv) erasing said memory circuit ~~and (v) programming said programmable logic device~~.